FPGA Development Board AX301

User Manual

ALINX

Version Record

Revision	Date	Release By	Description
Rev 1.0	2020-01-01	Rachel Zhou	First Release

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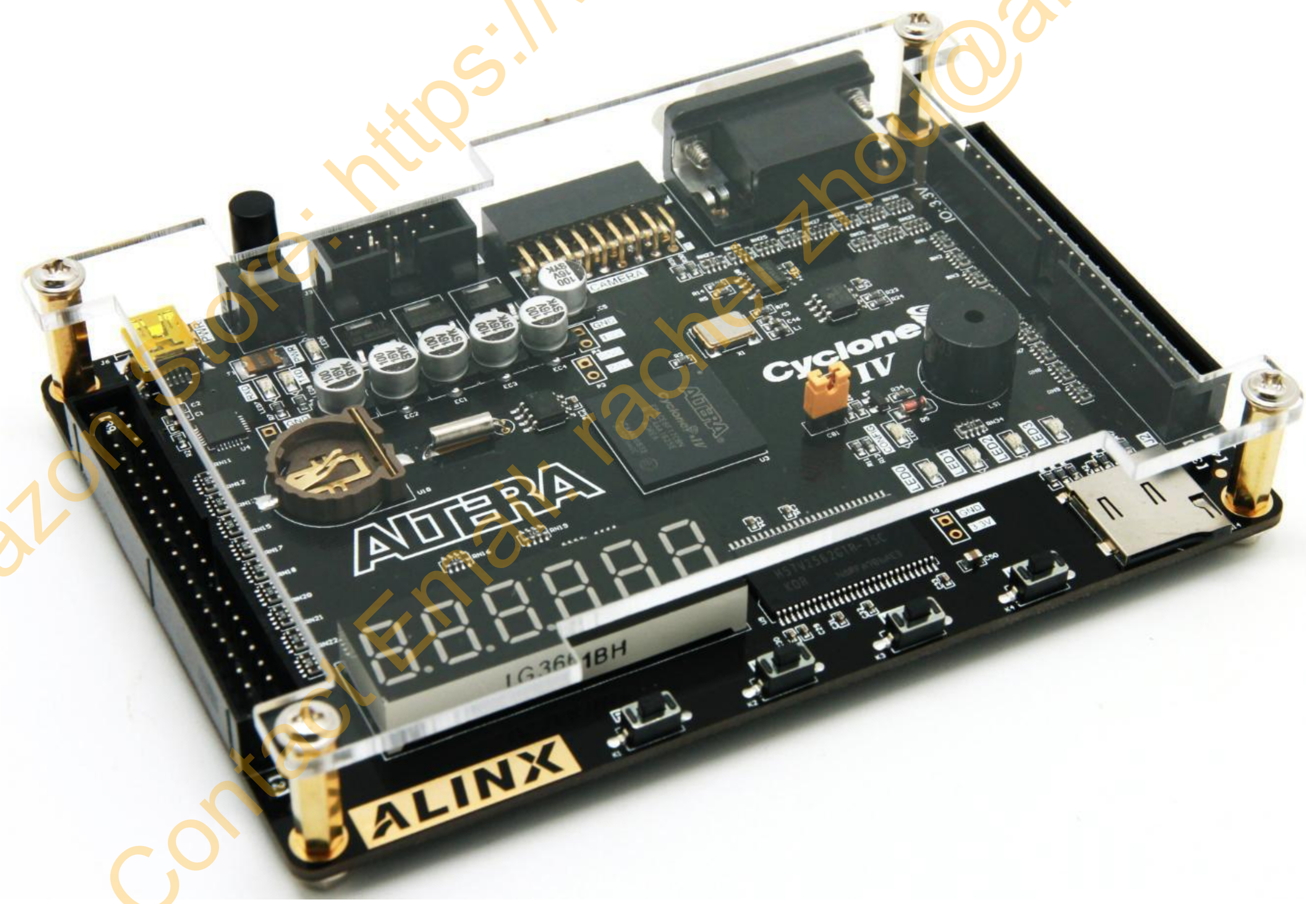
The ALINX AX301 development board is an entry-level product for ALTERA FPGAs and is primarily targeted at FPGA beginners. AX301 uses ALTERA's Cyclone IV series chip, the model is EP4CE6F17C8, and it is a 256-pin FBGA package. The configuration of the entire development board is practical. There are two ALINX standard 40-pin 2.54 pitch expansion ports, a total of 34 * 2 = 68 IOs. In addition, 5V power, 3.3V power, and multiple GNDs are also available. It is a very good choice for DIY players. In addition, many ALINX supporting modules can also be directly connected to the expansion port of this FPGA development board, such as ADDA module, 4.3 inch LCD screen, audio module, camera, etc. provide more options. The following is a detailed introduction to AX301.



Part 1: FPGA Development Board Introduction

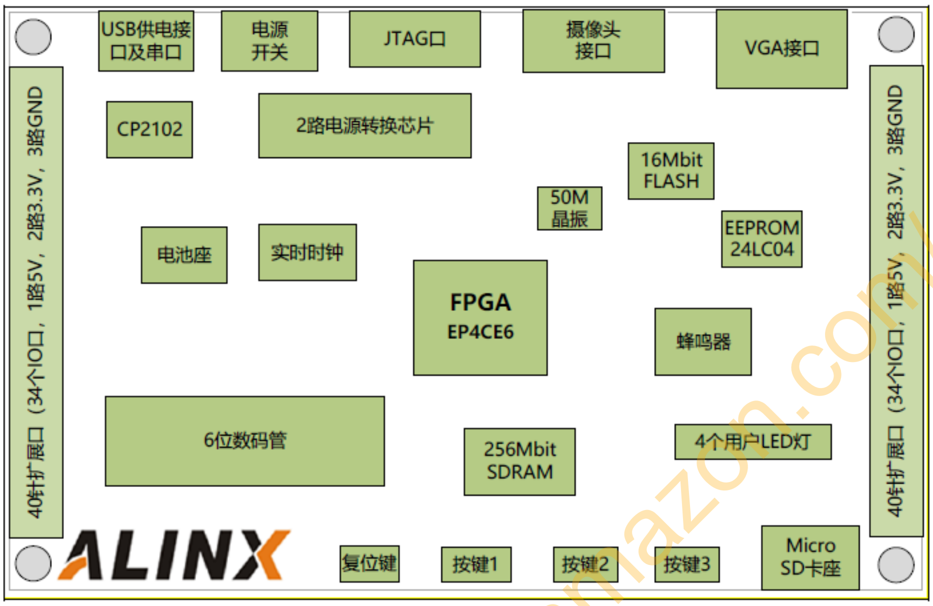
The AX301 development board uses ALTERA's Cyclone IV series FPGA, the model is EP4CE6F17C8, and a 256-pin FBGA package. The resources of this FPGA are shown below:

Resources	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Logic elements (LEs)	6,272	10,320	15,408	22,320	28,848	39,600	55,856	75,408	114,480
Embedded memory (Kbits)	270	414	504	594	594	1,134	2,340	2,745	3,888
Embedded 18 × 18 multipliers	15	23	56	66	66	116	154	200	266
General-purpose PLLs	2	2	4	4	4	4	4	4	4
Global Clock Networks	10	10	20	20	20	20	20	20	20
User I/O Banks	8	8	8	8	8	8	8	8	8
Maximum user I/O (1)	179	179	343	153	532	532	374	426	528

The main parameters as below:

Parameters	Value
Logic elements(LEs)	6272
Embedded memory(Kbits)	270
Embedded 18x18multipliers	15
Global Phase Locked Loop (PLLs)	2
Global Clock Networks	10
Maximum number of available IOs	179
Core voltage	1.15V-1.25V(recommend 1.2V);
Operating temperature	0-85℃

The structure of the entire system is shown in Figure 1-1:



Through the diagram, we can see the functions that the development platform can achieve:

- USB interface power supply, and realize USB to serial port function
- A large-capacity 256Mbit SDRAM can be used as data cache
- A 16Mbit SPI FLASH can be used as FPGA configuration file and user data storage
- One camera interface for 5 million OV5640 camera module
- One VGA interface, VGA interface is 16bit, can display 65536 colors, can display color pictures and other information
- One piece of RTC real-time clock, equipped with a battery holder, the battery model is CR1220
- One EEPROM 24LC04 with IIC interface
- 4 red LEDs, can realize the function of running light
- 4 buttons, 1 reset button, 3 user button
- 50M active crystal on board, providing stable clock source for development board
- Two 40-pin ALINX standard expansion ports (2.54mm pitch), of which 34 IO ports, one 5V power supply, two 3.3V power supplies, and three GND. Two expansion modules can be connected at the same time,

such as 4.3-inch TFT module and AD / DA module

- The JTAG port is reserved for debugging and program curing of the FPGA.
- 1 Micro SD card slot, support SPI mode One 6-digit digital tube, can display 6 digits dynamically

Part 2: Power Supply

The AX301 development board is powered by USB. Use a MINI USB cable to connect the development board to the computer's USB and press the power switch to power the development board. The power supply design diagram of the development board is as Figure 2-1:

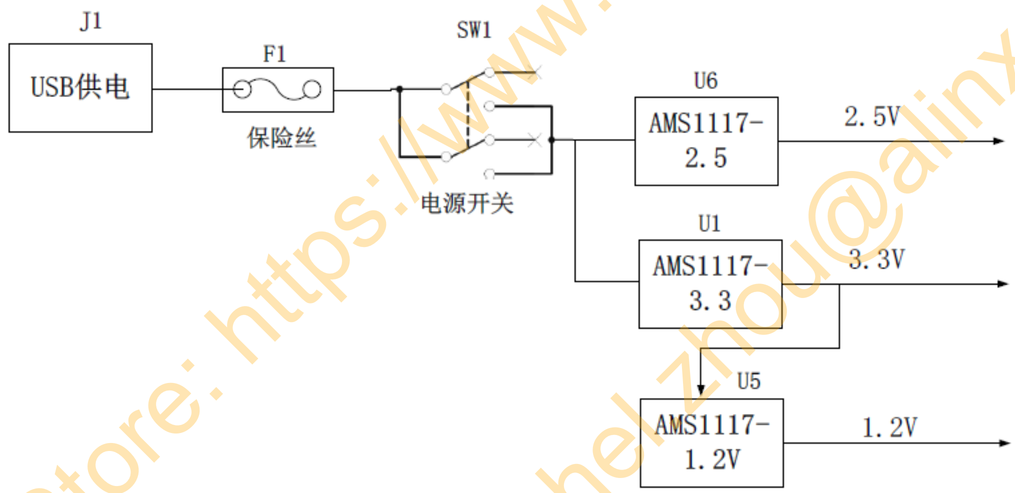


Figure 2-1: Power Supply Schematic

The development board is powered by USB and generates three power sources: + 3.3V, + 2.5V, and + 1.2V through three LDO power chips to meet the bank voltage and core voltage of the FPGA.

In the PCB design, a 4-layer PCB is used, and a separate power supply layer and GND layer are reserved, so that the power supply of the entire development board has very good stability. Test points for each power supply are reserved on the PCB so that the user can confirm the voltage on the board.

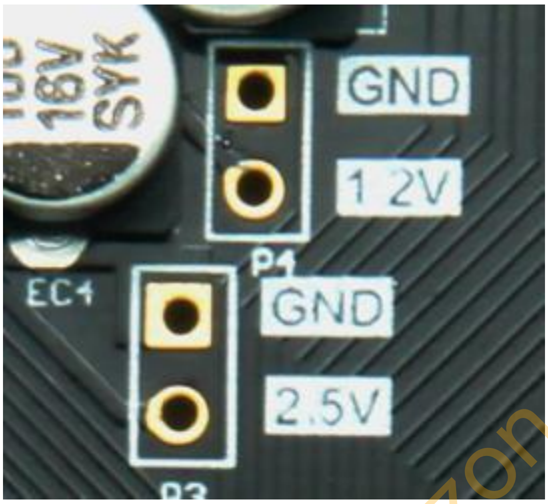


Figure 2-2: Test Points for Power supply on the Board

Part 3: FPGA

The FPGA model used by the AX301 development board is EP4CE6F17C8, which belongs to ALTERA's Cyclone IV. This model is a BGA package with 256 pins. The definition of FPGA pins is explained again. Many people use FPGAs that are non-BGA packages, such as 144-pin, 208-pin FPGA chips. Their pin definitions are composed of numbers, such as 1 to 144, 1 to 208, and so on. When we use a BGA packaged chip, the pin names become **letters + numbers**, such as E3, G3, etc. Therefore, when reading the schematic diagram, the letters + numbers in this form represent the FPGA Pin. Having said this, let's look at the functions of various parts related to FPGA. Figure 3-1 is the FPGA chip used in the development board.

Figure 3-1: The FPGA chip on the Board

Part 3.1: JTAG Interface

First of all, let's talk about the configuration and debugging interface of FPGA: JTAG interface. The function of the JTAG interface is to download the compiled program (.sof) into the FPGA or the FLASH configuration program (.jic) to the SPI FLASH. After the sof file is downloaded to the FPGA, it will be lost after power failure. You need to power on and download again. At this time, we can convert the sof file into a jic file through the Quartus software. After downloading the jic file to the development board's FLASH through JTAG, it will not be lost after power off, and the FPGA will read the jic configuration file in FLASH and run after power on again.

Figure 3-2 is the schematic part of the JTAG port, which involves the four signals TCK, TDO, TMS, TDI. These four signals are directly derived from the FPGA pins, and each signal has a diode overvoltage protection circuit on the development board.

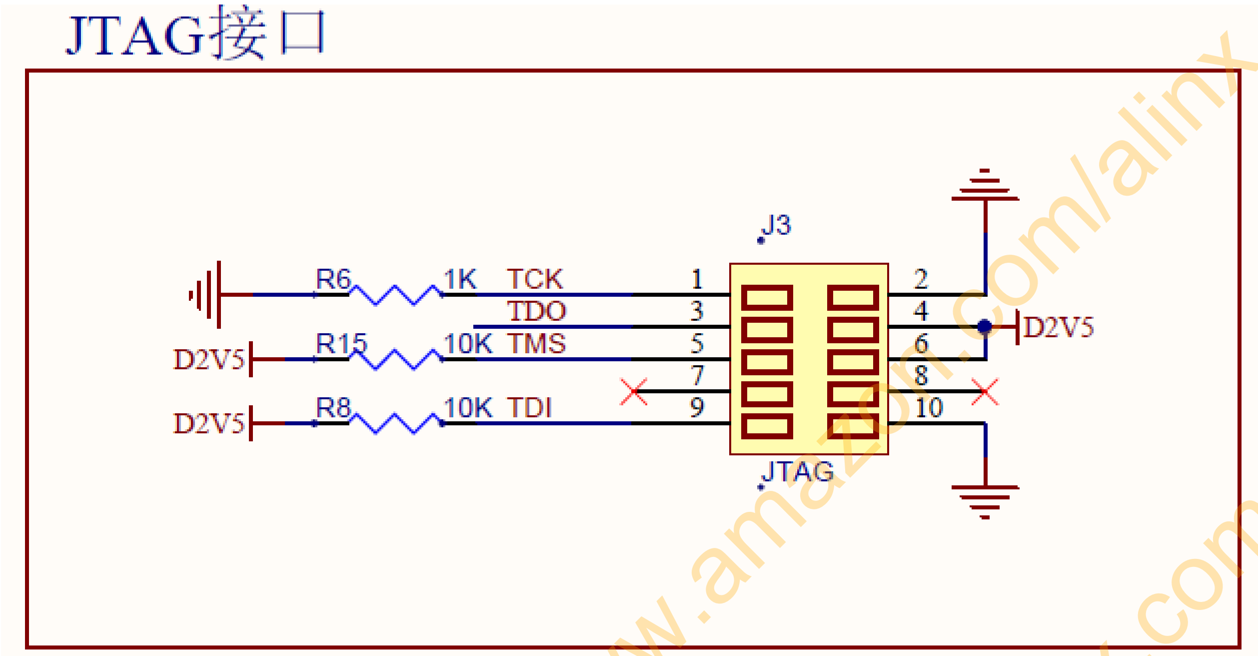


Figure 3-2: The JTAG port schematic

The JTAG interface uses a 10-pin 2.54mm standard connector. Figure 3-3 is the JTAG interface on the development board.

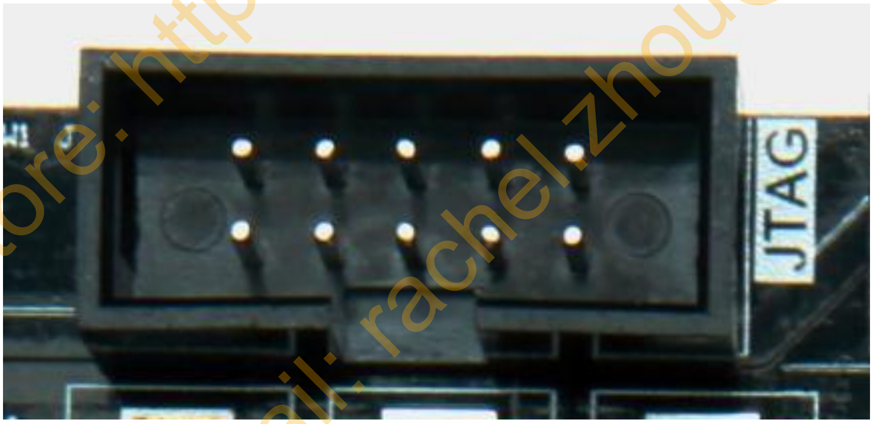


Figure 3-3: The JTAG port on the FPGA Board

Part 3.2: FPGA power and GND pins

Next, let's talk about the power pins of the FPGA. It includes the power supply pin, core voltage pin, analog voltage and phase-locked loop power supply pin of each bank. VCCINT is the FPGA core power supply pin, which is connected to 1.2V. VCCIO is the power supply voltage of each bank of the

FPGA. Among them, VCCIO0 is the power supply pin of FPGA BANK0. Similarly, VCCIO1 ~ VCCIO3 are the power supply pins of FPGA BANK ~ BANK3 respectively. In the development board, VCCIO is connected to 3.3V voltage. Both pins are 3.3V input and output. VCCA is the FPGA analog power supply pin, which is connected to 2.5V, VCCD_PLL is the FPGA phase-locked loop power supply pin, and also connected to 1.2V. The power connection diagram of the FPGA chip is shown in Figure 3-4.

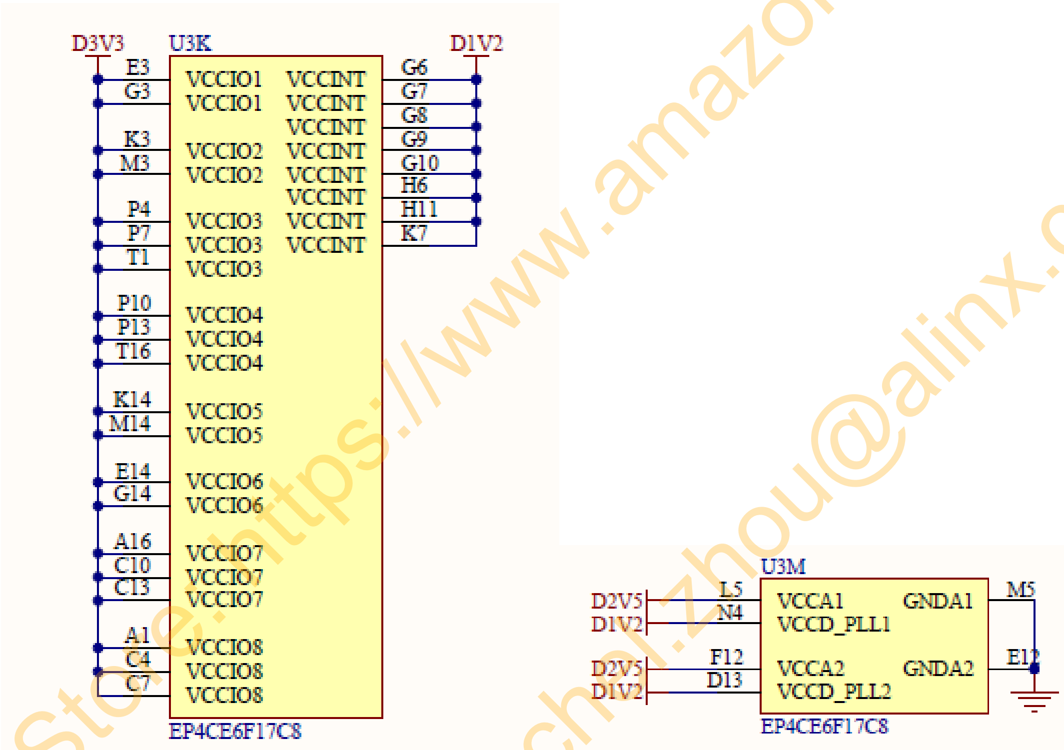


Figure 3-4: FPGA power pins

In addition, there are many pins on the FPGA that need to be connected to GND to ensure a stable ground reference inside the FPGA. The GND connected to the FPGA is shown in Figure 3-5

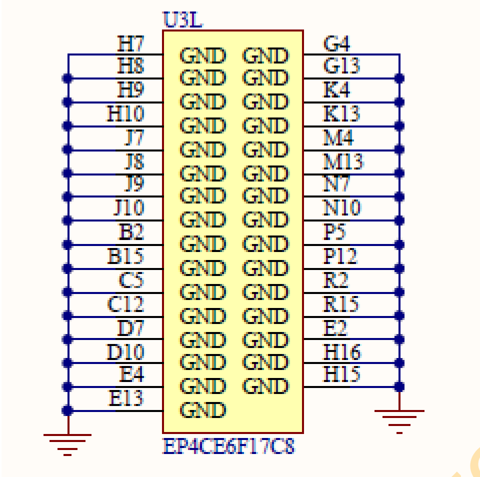


Figure 3-5: FPGA GND Pin

Part 4: 50M Active Crystal

Figure 4-1 is a 50M active crystal circuit that provides a clock source for the development board. Crystal output is connected to FPGA global input clock pin (CLK1 pin E1). This CLK1 can be used to drive the user logic circuit in the FPGA. The user can configure the FPGA's internal PLL (Phase Locked Loop) to divide and multiply to achieve clocks of other frequencies.

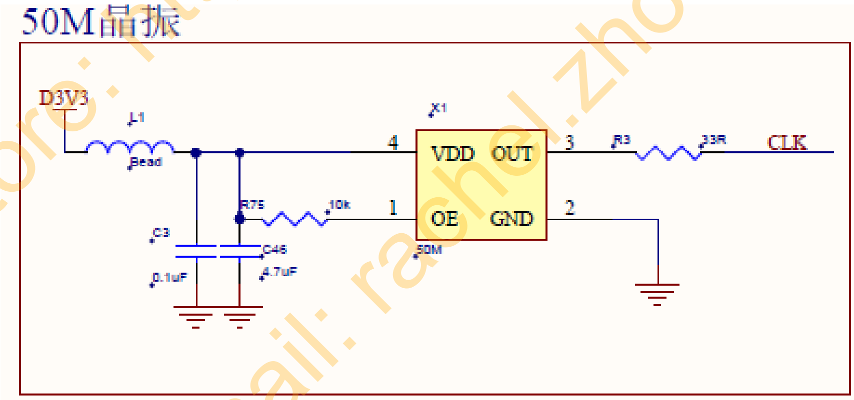


Figure 4-1: 50M Active Crystal Circuit

Figure 4-2: 50M Active Crystal on the FPGA Board

Clock pin assignment:

Pin Name	FPGA Pin
CLK	E1

Part 5: SPI Flash

The AX301 FPGA development board is equipped with a 16Mbit SPI FLASH chip, model W25P16, which uses the 3.3V CMOS voltage standard and completely replaces the configuration chip EPCS16 of ALTERA. Due to its non-volatile characteristics, in use, SPI FLASH can be used as the boot image of the FPGA system. These images mainly include the JIC configuration files for the FPGA, soft application code, and other user data files.

The specific model and related parameters of SPI FLASH are shown in Table 5-1.

Position	Model	Capacity	Factory
U8	W25P16	16M Byte	ST

Table 5-1: SPI FLASH Specification

The SPI Flash schematic is shown in Figure 5-2

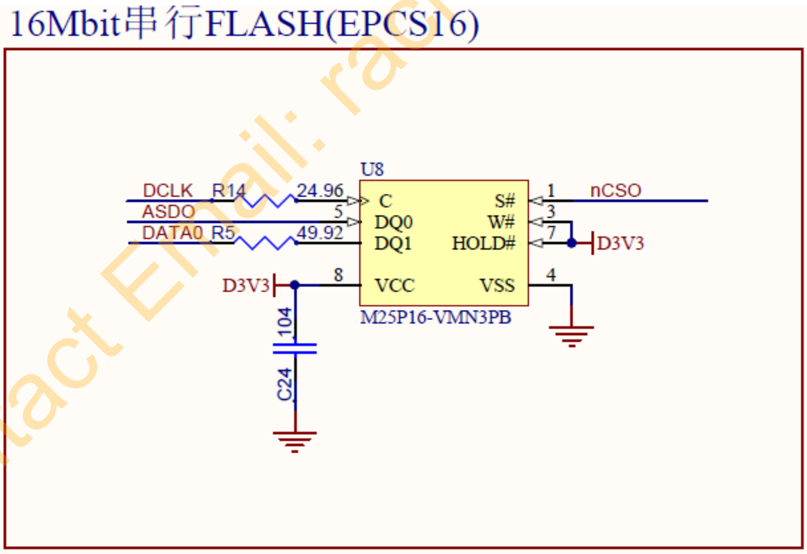


Figure 5-1: SPI Flash Connection Diagram

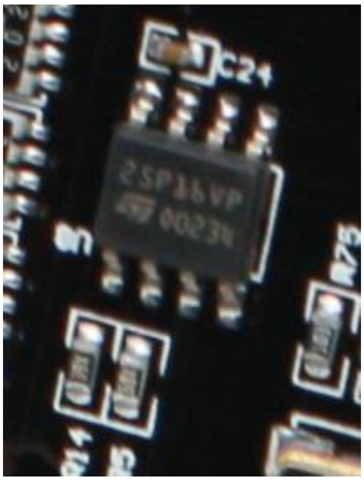


Figure 5-2: SPI Flash on the FPGA Board

Configure chip pin assignments:

Pin Name	FPGA Pin
DCLK	H1
nCSO	D2
DATA0	H2
ASDO	C1

Part 6: SDRAM

The AX301 FPGA development board has an SDRAM chip on board, model: HY57V2562GTR, capacity: 256Mbit (16M * 16bit), 16bit bus. SDRAM can be used for data buffering. For example, the data collected by the camera is temporarily stored in SDRAM and then displayed through the VGA interface. Here SDRAM is used for data caching.

The hardware connection of SDRAM is shown in Figure 6-1

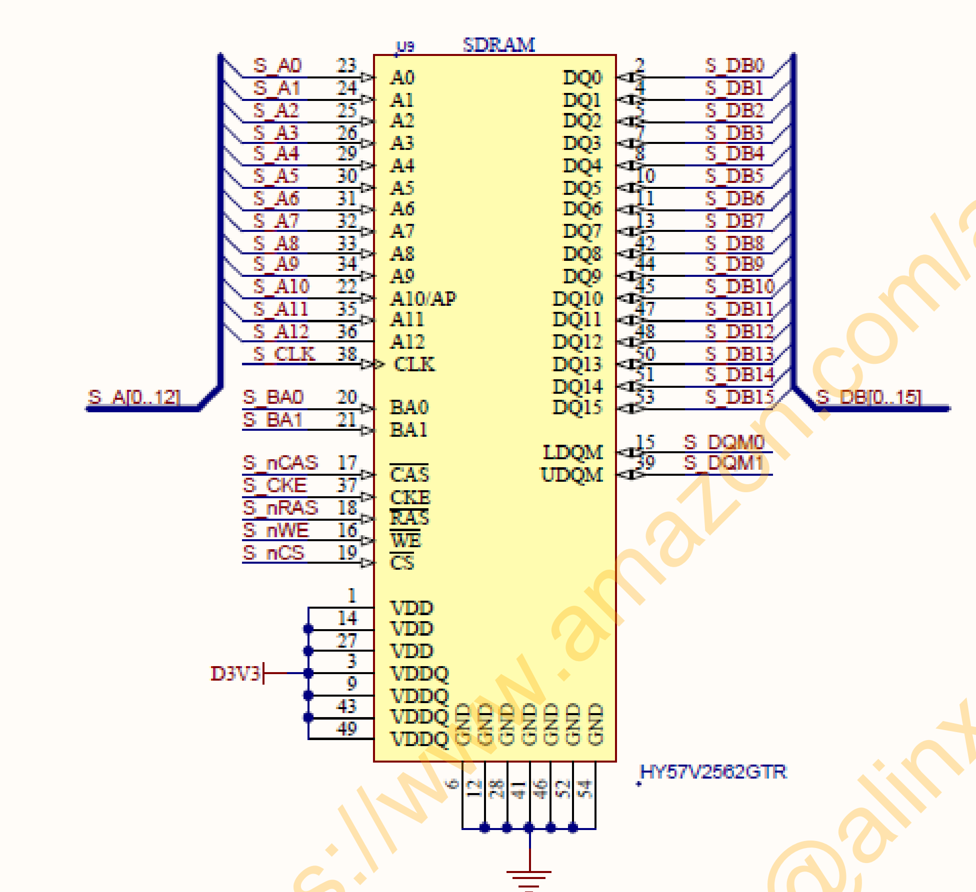


Figure 6-1: SDRAM schematic

Figure 6-2: SDRAM on the FPGA Board

SDRAM pin assignment:

Pin Name	FPGA Pin
S_CLK	B14
S_CKE	F16
S_NCS	K10
S_NWE	J13
S_NCAS	J12
S_NRAS	K11
S_DQM<0>	J14
S_DQM<1>	G15
S_BA<0>	G11
S_BA<1>	F13
S_A<0>	F11
S_A<1>	E11
S_A<2>	D14
S_A<3>	C14
S_A<4>	A14
S_A<5>	A15
S_A<6>	B16
S_A<7>	C15
S_A<8>	C16
S_A<9>	D15
S_A<10>	F14
S_A<11>	D16
S_A<12>	F15
S_DB<0>	P14
S_DB<1>	M12
S_DB<2>	N14
S_DB<3>	L12
S_DB<4>	L13
S_DB<5>	L14
S_DB<6>	L11
S_DB<7>	K12
S_DB<8>	G16

S_DB<9>	J11
S_DB<10>	J16
S_DB<11>	J15
S_DB<12>	K16
S_DB<13>	K15
S_DB<14>	L16
S_DB<15>	L15

Part 7: EEPROM 24LC04

AX301 FPGA development board contains an EEPROM, model 24LC04, and has a capacity of 4Kbit (2*256*8bit). It consists of two 256-byte blocks and communicates via the IIC bus. The EEPROM is generally used in the design of instruments and meters, and is used to store some parameters. This kind of chip is easy to operate and has a very high price-performance ratio, so although the capacity ratio is high, the price is very cheap. It is a good choice for those products that require high cost. Figure 7-1 is the schematic diagram of EEPROM

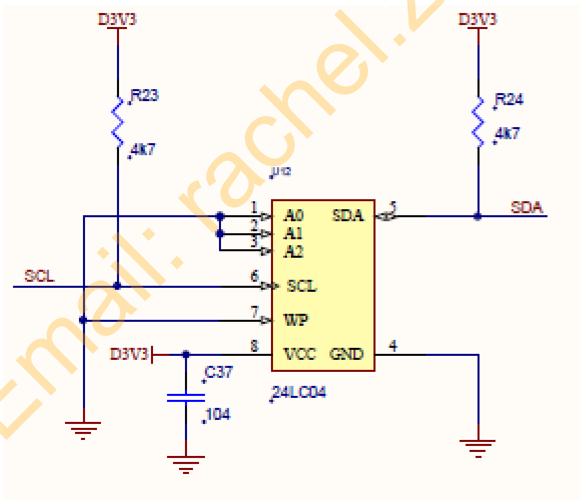


Figure 7-1: EEPROM Schematic

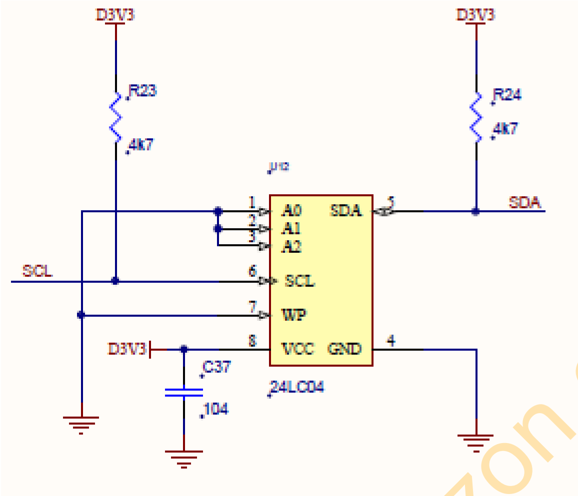


Figure 7-2: EEPROM on the FPGA Board

EEPROM Pin Assignment

Pin Name	FPGA Pin
SDA	E6
SCL	D1

Part 8: Real-time clock DS1302

The AX301 FPGA development board contains a real-time clock RTC chip, model DS1302, which provides a calendar function up to 2099, with days, minutes, minutes, seconds and weeks. If time is needed in the system, then the RTC needs to be involved in the product. It needs to connect a 32.768KHz passive clock to provide an accurate clock source to the clock chip, so that the RTC can accurately provide clock information to the product. At the same time, in order to power off the product, the real-time clock can still operate normally. Generally, a battery is required to supply power to the clock chip. In Figure 8-1, the U10 is the battery holder, and the button battery (model CR1220, voltage is 3V) is placed. After the system is turned off, the button battery can also supply power to the DS1302. This way, regardless of whether the product is powered or not, the DS1302 will operate normally without interruption and provide continuous time information. Figure 8-1 shows the design of the DS1302:

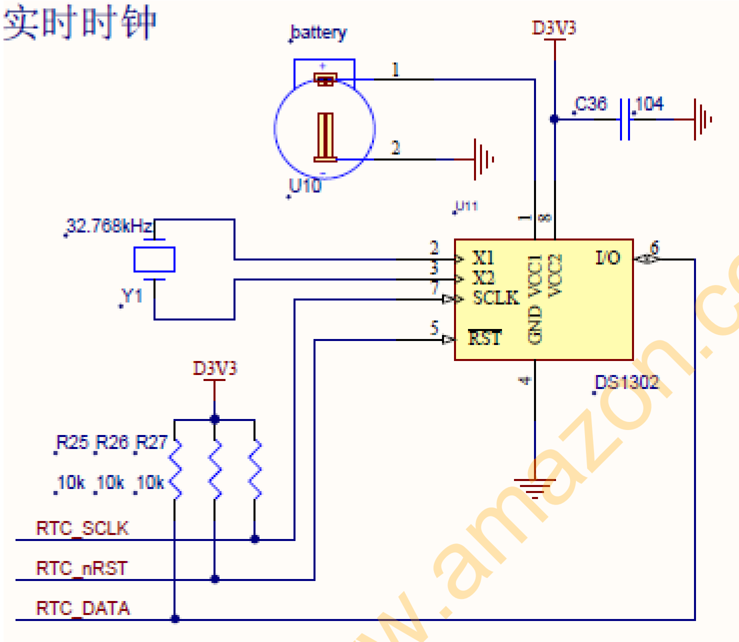


Figure 8-1: DS1302 schematic

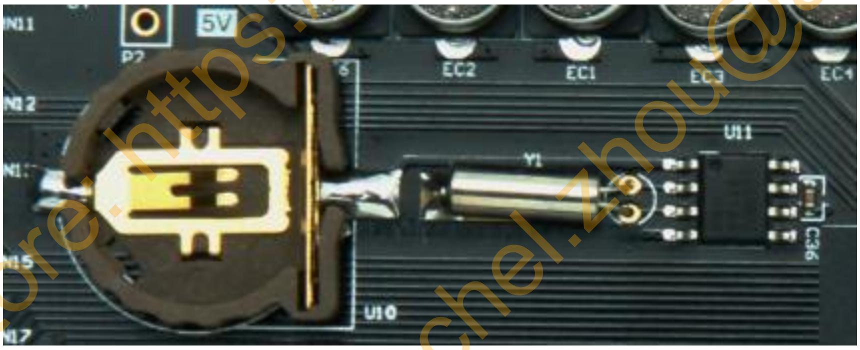


Figure 8-12: DS1302 on the FPGA Board

DS1302 interface pin assignment:

Pin Name	FPGA Pin
RTC_SCIK	P6
RTC_nRST	N8
RTC_DATA	M8

Part 9: USB to Serial Port

The development board contains the Silicon Labs CP2102GM USB-UAR chip. The USB interface uses the MINI USB interface. This USB interface implements the power supply function, and it can implement the USB to serial port function. You can use a USB cable to connect it to the USB port of the PC for serial data communication.

The schematic diagram of the serial port is shown in Figure 9-1

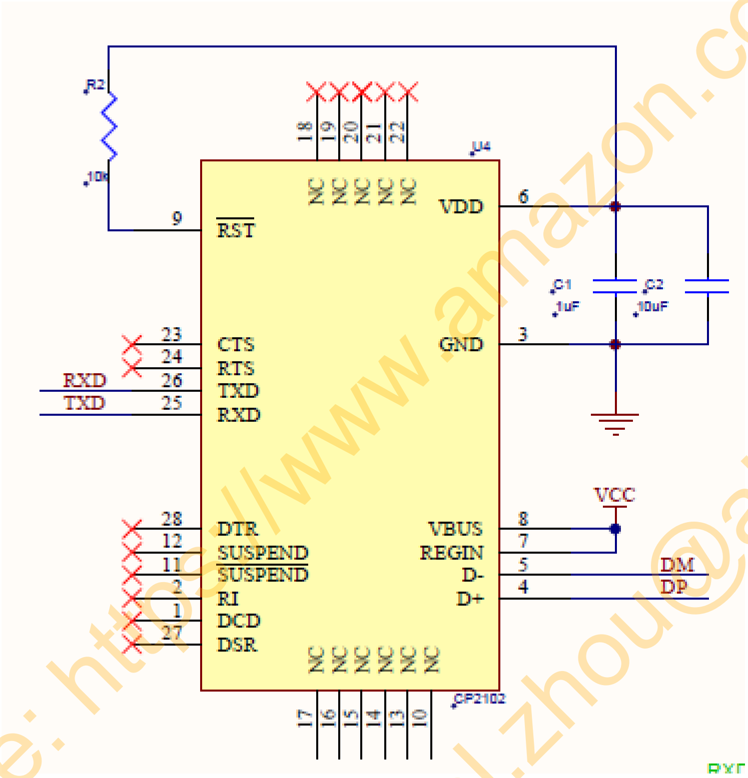


Figure 9-1: USB to serial port schematic

Figure 9-2: USB to serial port on the FPGA Board

At the same time, two led indicators (LED7, LED8) are set for the serial port signal. LED7 and LED8 will indicate whether there is data transmitted or received by the serial port, as shown in Figure 9-3.

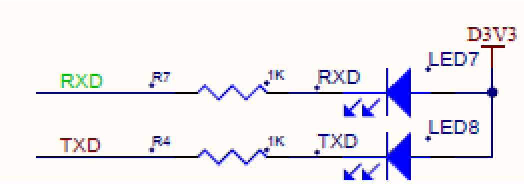


Figure 9-3: USB to serial port signal indicator

USB to serial port pin assignment:

Pin Name	FPGA Pin
RXD	M2
TXD	N1

Part 10: VGA Interface

The VGA interface is the main interface on computer monitors. Since the era of CRT displays, the VGA interface has been used and has been in use ever since. The VGA interface is also called the D-Sub interface.

The VGA interface is a D-type interface with a total of 15 pinholes divided into three rows of five. What is more important are the 3 RGB color component signals and the 2 scanning synchronization signals HSYNC and VSYNC pins.

Pins 1, 2, and 3 are analog voltages of three primary colors: red, green, and blue. They are 0 to 0.714V peak-peak. 0V means colorless, and 0.714V means full color. Some non-standard displays use a full color level of 1Vpp.

The three primary color source terminals and termination matching resistors are 75 ohms. Detailed as Figure 10-1:

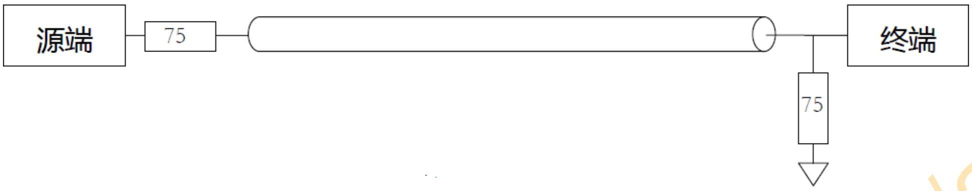


Figure 10-1: VGA video signal transmission diagram

HSYNC and VSYNC are line data synchronization and frame data synchronization, respectively, and are TTL levels. FPGA can only output digital signals, and R, G, and B required by VGA are analog signals. The digital-to-analog signals of VGA are implemented by a simple resistor circuit. This resistor circuit can generate 32 gradient levels of red and blue signals and 64 gradient levels of green signals (RGB 5-6-5). The VGA interface circuit is shown in Figure 10-2.

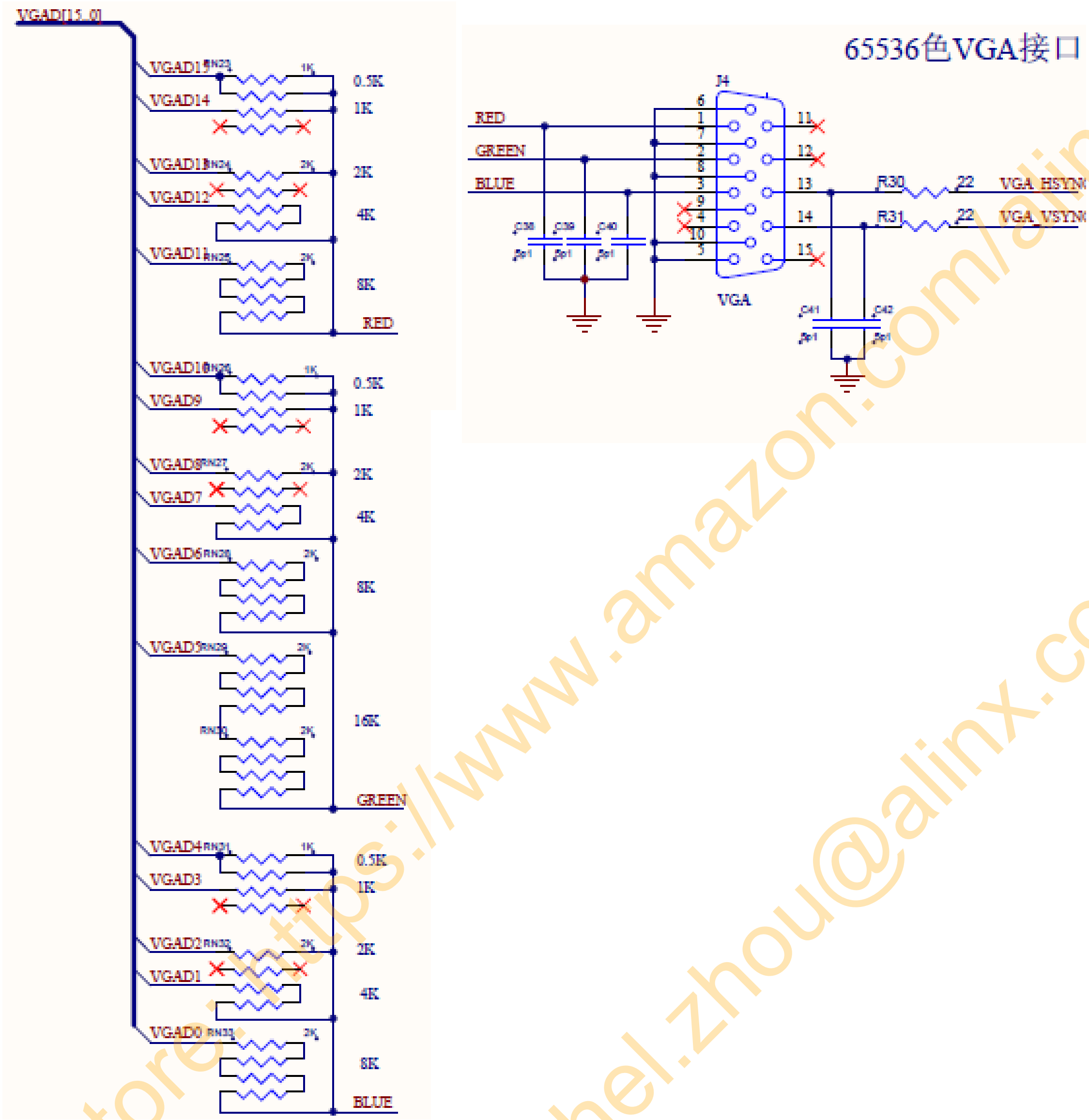


Figure 10-2: VGA Interface Schematic

Figure 10-3: VGA Interface on the FPGA Board

VGA interface pin assignment

Pin Name	FPGA Pin	Description
VGA_D[0]	C3	BLUE[0]

VGA_D[1]	D4	BLUE[1]
VGA_D[2]	D3	BLUE[2]
VGA_D[3]	E5	BLUE[3]
VGA_D[4]	F6	BLUE[4]
VGA_D[5]	F5	GREEN[0]
VGA_D[6]	G5	GREEN[1]
VGA_D[7]	F7	GREEN[2]
VGA_D[8]	K8	GREEN[3]
VGA_D[9]	L8	GREEN[4]
VGA_D[10]	J6	GREEN[5]
VGA_D[11]	K6	RED[0]
VGA_D[12]	K5	RED[1]
VGA_D[13]	L7	RED[2]
VGA_D[14]	L3	RED[3]
VGA_D[15]	L4	RED[4]
VGA_HS	L6	Line sync signal
VGA_VS	N3	Field sync signal

Part 11: SD Card Slot

SD card (Secure Digital Memory Card) is a kind of memory card based on semiconductor flash memory technology. In 1999, it was led by Panasonic in Japan. Participants Toshiba and SanDisk Corporation in the United States carried out substantial research and development to complete it. In 2000, these companies initiated the establishment of the SD Association (Secure Digital Association for short), which has a strong lineup and attracted a large number of manufacturers to participate. These include IBM, Microsoft, Motorola, NEC, Samsung, etc. Driven by these leading manufacturers, SD card has become the most widely used memory card in consumer digital devices.

SD card is a very common storage device now. The SD card we extended supports SPI mode. The SD card used is a MicroSD card. The schematic is shown in Figure 11-1.

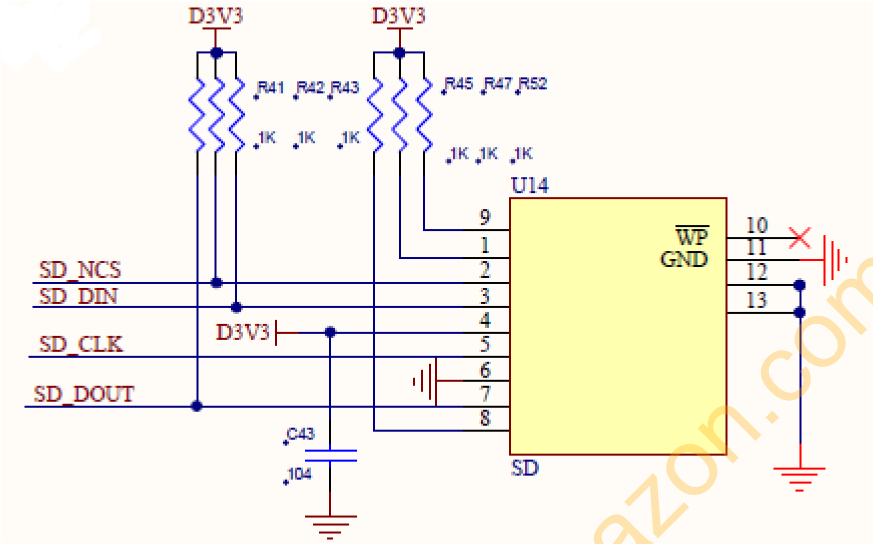


Figure 11-1: SD card slot schematic

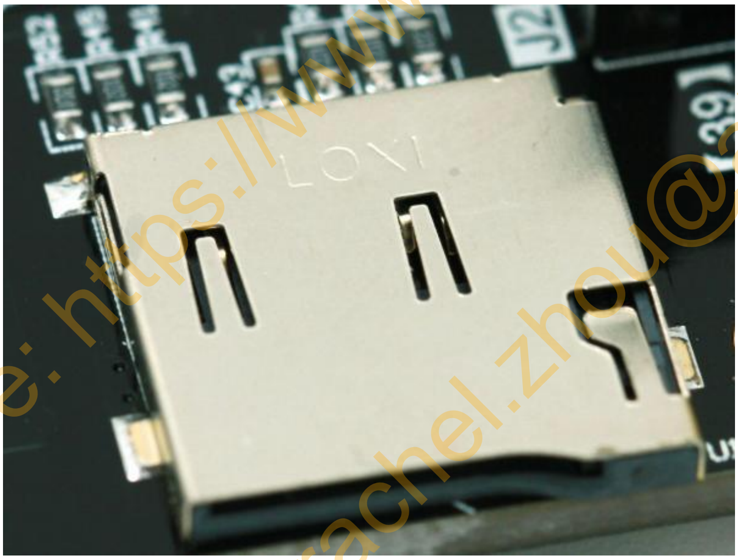


Figure 11-2: SD card slot on the FPGA Board

SD card slot pin assignment

SD Mode	
Pin Name	FPGA Pin
SD_NCS	D11
SD_DIN	F10
SD_CLK	D12
SD_DOUT	E15

Part 12: LEDs

The AX301 FPGA development board has 4 user LEDs on board. The schematic diagram of the four user LEDs is shown in Figure 12-1. When the FPGA pin output is logic 0, the LEDs will off. When the output is logic 1, the LED is lit.

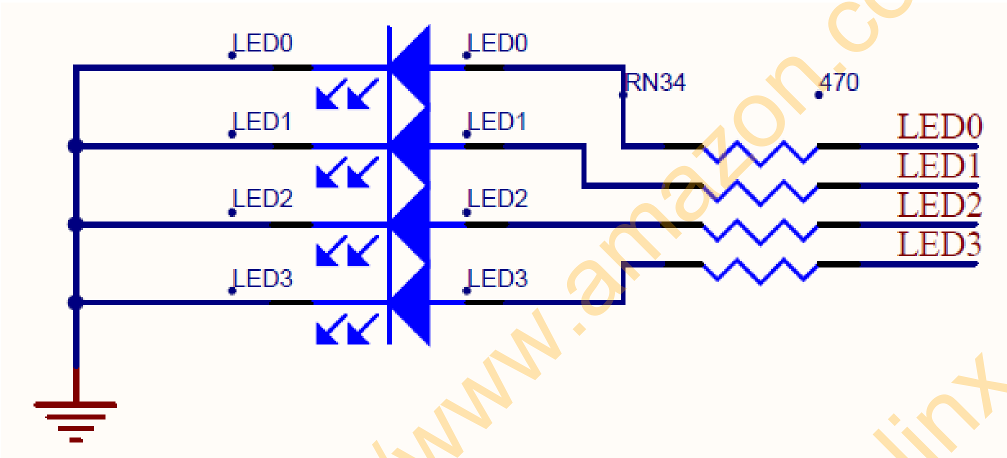


Figure 12-1: User LEDs Schematic

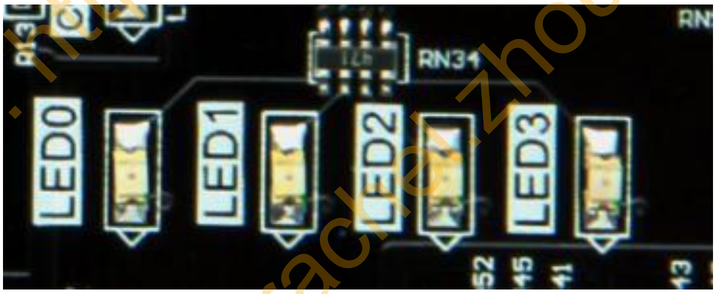


Figure 12-2: User LEDs on the FPGA Board

LEDs pin assignment:

Pin Name	FPGA Pin
LED0	E10
LED1	F9
LED2	C9
LED3	D9

Part 13: User Keys

The development board has 4 independent keys, 3 user keys (KEY1 ~ KEY3), and 1 function key (RESET). **Press the key to low level (0), release to high level (1).** The schematic diagram of the four keys is shown in Figure 13-1:

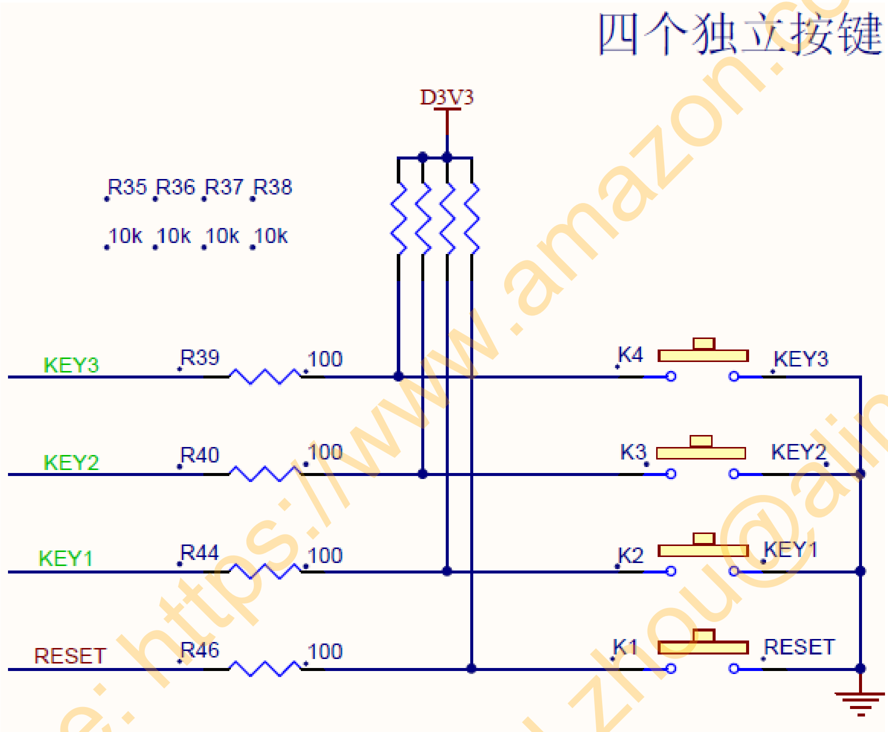


Figure 13-1: 4 user keys schematic

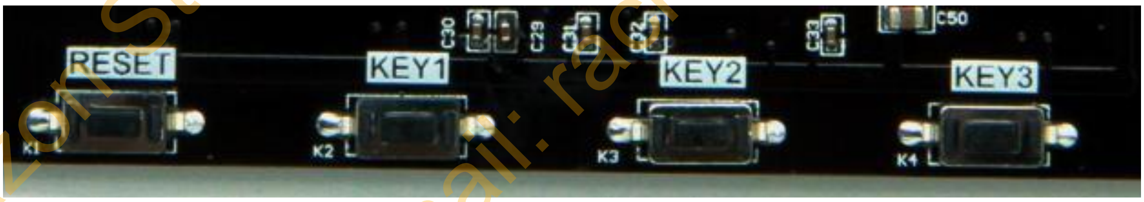


Figure 13-2: 4 users keys on the FPGA Board

Keys Pin assignment:

Key Name	FPGA Pin	Key Number
RESET	N13	RESET
KEY1	M15	KEY 1
KEY2	M16	KEY 2
KEY3	E16	KEY 3

Part 14: Camera Module interface

The development board includes an 18-pin CMOS camera interface, which can be connected to the OV5640 camera module to implement the video capture function. After the capture, the display can be connected to the display through a TFT LCD screen or a VGA interface. Regarding the camera selection, users can choose according to their actual needs.

The CMOS camera interface schematic is shown in Figure 14-1

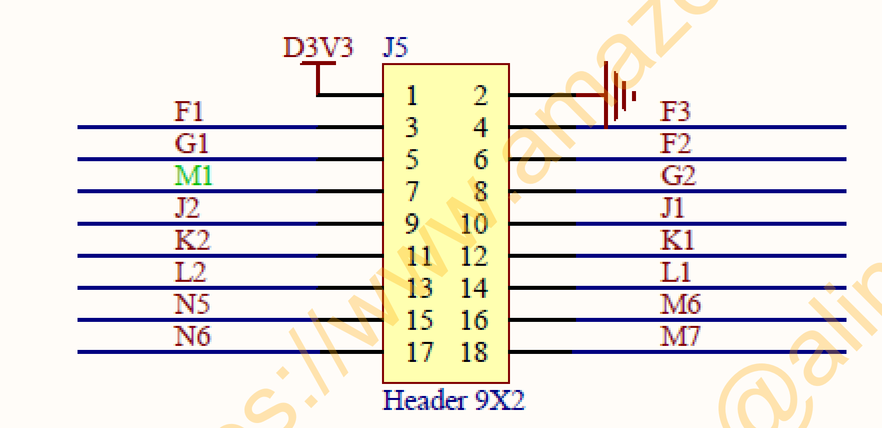


Figure 14-1: Camera Interface Schematic

Figure 14-2: Camera Interface on the FPGA Board

(The camera module is optional and needs to be purchased separately)

Camera interface pin assignment:

Pin Number	FPGA Pin	OV5640 camera module
PIN1	+3.3V	+3.3V
PIN2	GND	GND
PIN3	F1	CMOS_SCL
PIN4	F3	CMOS_SDA
PIN5	G1	CMOS_PCLK
PIN6	F2	CMOS_VSYNC
PIN7	M1	CMOS_D3
PIN8	G2	CMOS_D2
PIN9	J2	CMOS_D7
PIN10	J1	CMOS_D6
PIN 11	K2	CMOS_XCLK
PIN 12	K1	CMOS_HREF
PIN 13	L2	CMOS_D0
PIN 14	L1	CMOS_D4
PIN 15	N5	CMOS_D5
PIN 16	M6	CMOS_D1
PIN 17	N6	CMOS_RESET
PIN 18	M7	CMOS_PWDN

Part 15: Digital Tube

Nixie tube is a very common display device, generally divided into seven-segment digital tube and eight-segment digital tube. The difference between the two is that the eight-segment digital tube has one more "dot" than the seven-segment digital tube. The digital tube we use is a six-in-one eight-segment digital tube. The digital tube segment structure is shown in Figure 15-1:

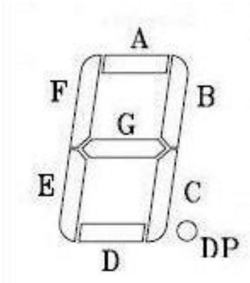


Figure 15-1: Digital tube segment structure

We use a common anode digital tube. **When the pin corresponding to a field is low, the corresponding field is lit, and when the pin corresponding to a field is high, the corresponding field is not lit.**

Having said the schematic diagram above, let's look at the design on FPGA development board.

The six-in-one digital tube is a dynamic display. Due to the persistence of human vision and the afterglow effect of light emitting diodes, although the digital tubes are not lit at the same time, as long as the scanning speed is fast enough, the impression is a group Stable display data without flickering.

The same sections of the six-in-one digital tube are connected together, with a total of 8 pins, and then 6 control signal pins are added, and a total of 14 pins, as shown in Figure 15-2. Among them DIG [0..7] is A, B, C, D, E, F, G, H (ie point DP) corresponding to the digital tube; SEL [0..5] is the six controls of the six digital tubes The pin is also active low. When the control pin is low, the corresponding digital tube has a power supply voltage so that the digital tube can light up. Otherwise, no matter how the segment of the nixie tube changes, the corresponding nixie tube cannot be lighted.

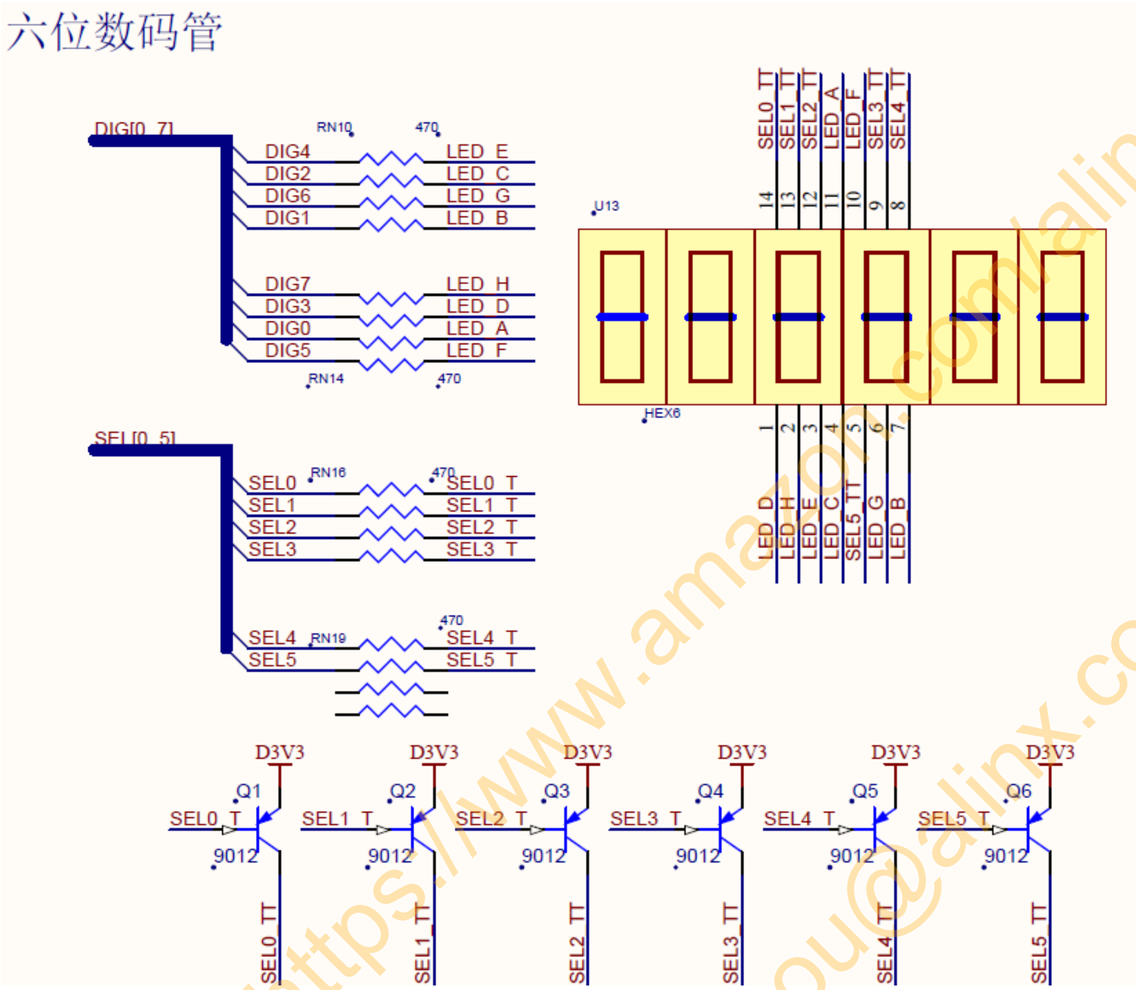


Figure 15-2: Digital tube schematic

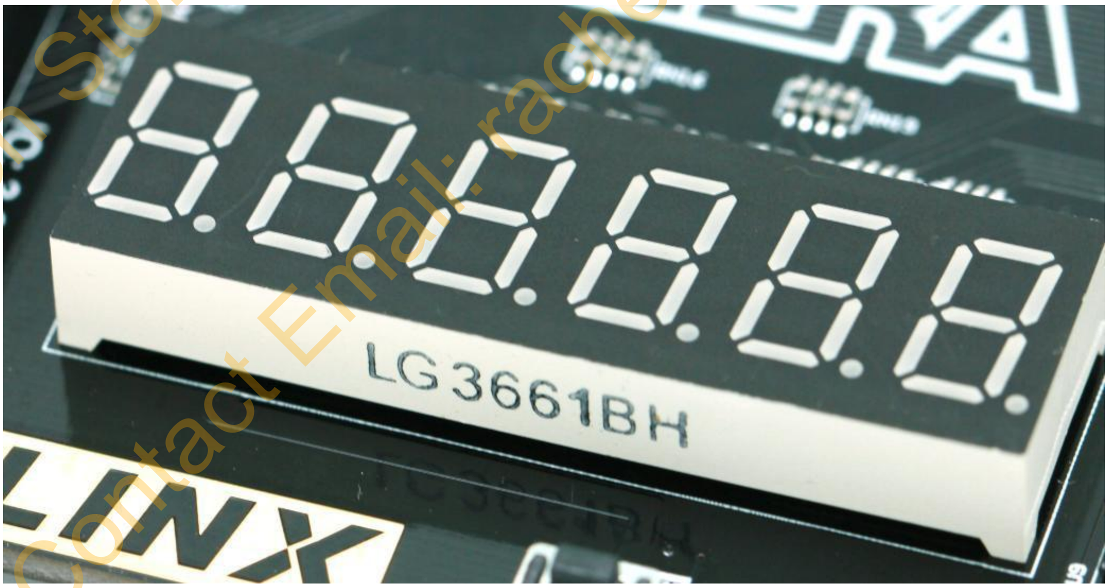


Figure 15-3: Digital tube on the FPGA Board

Digital tube pin assignment

Pin Name	FPGA Pin	Description
DIG[0]	R14	Corresponding section A
DIG[1]	N16	Corresponding section B
DIG[2]	P16	Corresponding section C
DIG[3]	T15	Corresponding section D
DIG[4]	P15	Corresponding section E
DIG[5]	N12	Corresponding section F
DIG[6]	N15	Corresponding section G
DIG[7]	R16	Corresponding section DP
SEL[0]	N9	The first digital tube on the right
SEL[1]	P9	The second digital tube on the right
SEL[2]	M10	The third digital tube on the right
SEL[3]	N11	The fourth digital tube on the right
SEL[4]	P11	The fifth digital tube on the right
SEL[5]	M11	The sixth digital tube on the right

Part 16: Buzzer

The buzzer is controlled by a triode. When the level is low, the transistor is turned on and the buzzer sounds; when the level is high, the transistor is turned off and the buzzer does not sound. **For convenience, a jumper cap (CB1) is added between the buzzer and the FPGA. If you hate the buzzer, you can remove the jumper cap.** The schematic is shown in Figure 16.1

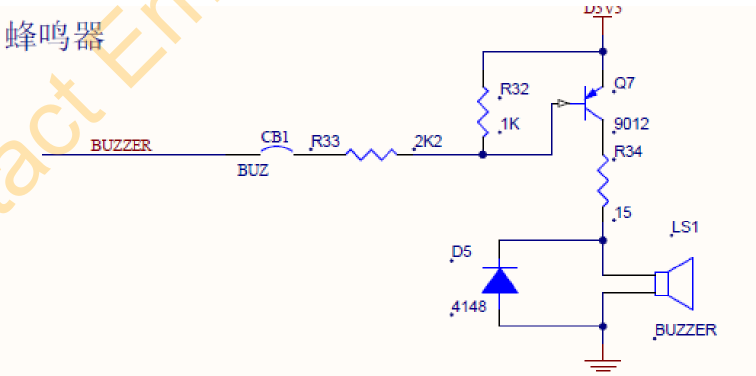


Figure 16-1: Buzzer schematic

Figure 16.-2 is the buzzer on the FPGA Development board. The yellow is the jumper connected to the buzzer and the FPGA pins. If you do not want the buzzer to sound, unplug it.

Figure 16-2: Buzzer schematic

Buzzer pin assignment:

Pin Name	FPGA Pin
Buzzer	C11

Part 17: Expansion Ports

The FPGA development board reserves 2 expansion ports, and the expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. These IO ports are independent IO ports and are not multiplexed with other devices. The IO port is connected to the FPGA pin and the level is 3.3V. **Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.**

The 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. The expansion ports (J1 and J2) circuits are shown in Figure 17-1 and Figure 17-2:

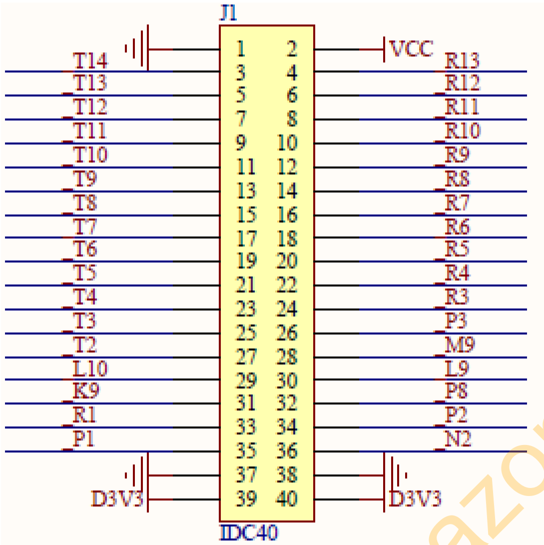


Figure 17-1: Expansion header J1 schematic

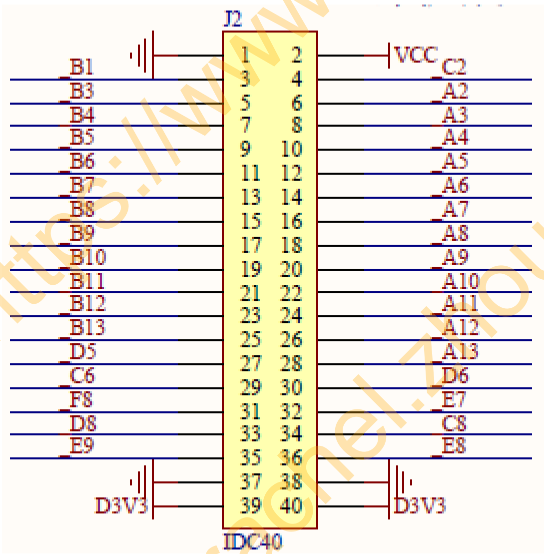


Figure 17-2: Expansion header J2 schematic

Figure 17-3 is the J1 and J2 expansion ports on the FPGA Development Board. Pin1, Pin2 and Pin39, Pin40 of the expansion ports have been marked on the board.

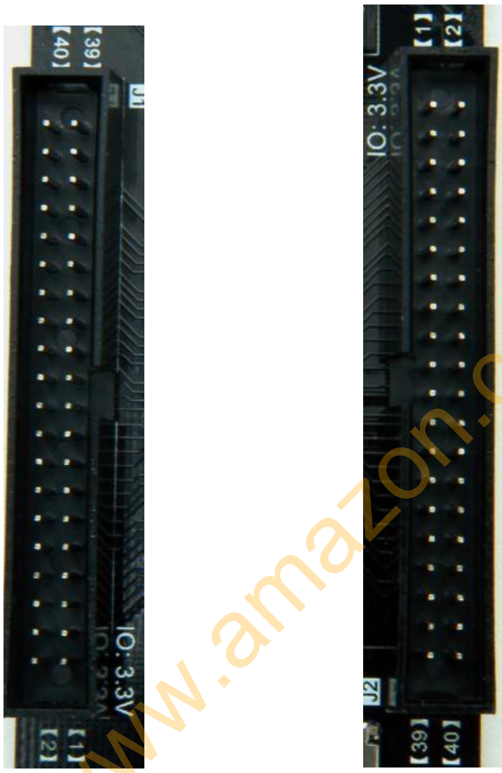


Figure 17-3: J1 and J2 expansion ports

J1 Expansion Header Pin Assignment

Pin Number	FPGA Pin	Pin Number	FPGA Pin
1	GND	**2**	VCC5V
3	T14	**4**	R13
5	T13	**6**	R12
7	T12	**8**	R11
9	T11	**10**	R10
11	T10	**12**	R9
13	T9	**14**	R8
15	T8	**16**	R7
17	T7	**18**	R6
19	T6	**20**	R5
21	T5	**22**	R4
23	T4	**24**	R3
25	T3	**26**	P3
27	T2	**28**	M9
29	L10	**30**	L9

31	K9	**32**	P8
33	R1	**34**	P2
35	P1		N2
37	GND	**38**	GND
39	D3V3	**40**	D3V3

J2 Expansion Header Pin Assignment

Pin Number	FPGA Pin	Pin Number	FPGA Pin
1	GND	**2**	VCC5V
3	B1	**4**	C2
5	B3	**6**	A2
7	B4	**8**	A3
9	B5	**10**	A4
11	B6	**12**	A5
13	B7	**14**	A6
15	B8	**16**	A7
17	B9	**18**	A8
19	B10	**20**	A9
21	B11	**22**	A10
23	B12	**24**	A11
25	B13	**26**	A12
27	D5	**28**	A13
29	C6	**30**	D6
31	F8	**32**	E7
33	D8	**34**	C8
35	E9	**36**	E8
37	GND	**38**	GND
39	D3V3	**40**	D3V3